What we claim as our invention is:

CLAIMS

[c1] 1. An apparatus to consolidate the output of data, the data comprising a plurality of data elements, the apparatus comprising:

a plurality of processors, each processor comprising:

an input register configured to receive a predetermined quantity of data elements;

at least one butterfly processor coupled to the input register, the butterfly processor configured to perform at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

at least one intermediate register coupled to the butterfly processor, the intermediate register configured to temporarily store the processed data; and

a feedback loop coupling the intermediate register and the butterfly processor, where if enabled, is configured to transfer a first portion of processed data elements to the appropriate butterfly processor to perform additional mathematical operations and, where if disabled, is configured to transfer a second portion of processed data elements to at least one holding register;

wherein the holding register is configured to store the processed data until all of the first portion data elements is processed; and

a plurality of output registers associated with the plurality of processors, wherein each output register is coupled to the holding register and another output register, each output register configured to receive the processed data from the holding register and route the processed data to an output register of a different processor.

[c2] 2. The apparatus set forth in Claim 1, further comprising at least one input multiplexer coupling the feedback loop and the intermediate register, wherein each input multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate butterfly processor.

[c3] 3. The apparatus set forth in Claim 1, further comprising at least one output multiplexer coupling the butterfly processor and the intermediate register, wherein each

output multiplexer is configured to temporarily select data elements and transfer data elements to the appropriate intermediate register.

[c4] 4. The apparatus set forth in Claim 1 wherein the block of encoded data may be represented as row data and column data, and further comprising a transpose random-access memory (RAM) coupled to the input register, wherein the transpose RAM is configured to store the row data while the column data is being processed, and wherein the transpose RAM is configured to store the column data while the row data is being processed.

[c5] 5. The apparatus set forth in Claim 4, wherein the transpose RAM is configurable to store two blocks of encoded data.

[c6] 6. The apparatus set forth in Claim 4, further comprising a write multiplexer coupling the holding register, wherein the write multiplexer is configured to resequence data elements to complete a one-dimensional transform.

[c7] 7. The apparatus set forth in Claim 1, wherein the data comprises a current group of data and a next group of data, the output registers are configured to operate on the current group of data simultaneous with the processor being configured to operate on a next group of data.

[c8] 8. The apparatus set forth in Claim 1, further comprising a control sequencer configured to control each processor.

[c9] 9. The apparatus set forth in Claim 8, where the control sequencer is configured to control each output register.

[c10] 10. The apparatus as set forth in Claim 1, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c11] 11. The apparatus set forth in Claim 1, wherein each output register is configured to saturate the processed data from seventeen bits to ten bits.

[c12] 12. In a system having a plurality of processors 1 to M, each processor having a corresponding output register 1 to N configurable to receive and transfer data, the data comprising a current group of data and a next group of data, each group comprising a plurality of portions of data, a method to transfer data comprising:

transferring the current group of data from each processor 1 to M its corresponding output register 1 to N;

receiving and processing the next group of data within each processor; and simultaneously,

transferring the portion of data from output register N to output register N-1, the portion of data from output register N-1 to output register N-2, and so on; and

transferring the portion of data from register 1 to a frame buffer.

[c13] 13. The method set forth in Claim 12, further comprising saturating each portion of the current group of data.

[c14] 14. The method as set forth in Claim 12, where M and N are 6.

[c15] 15. In a system having a plurality of processors 1 to M, each processor having a corresponding output register 1 to N configurable to receive and transfer data, a method to determine an inverse transform of a block of encoded data, the block of encoded data comprising a current group of data and a next group of data, each group comprising a plurality of data elements, the method comprising:

(a) receiving a predetermined quantity of data elements;

(b) performing at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

(c) making a determination as to whether any of the processed data elements require additional mathematical operations;

(d) selecting a first portion of processed data elements that require additional mathematical operations;

(e) selecting a second portion of processed data elements that do not require additional mathematical operations;

(f) performing at least one mathematical operation on selected pairs of the first portion of processed data elements to produce a second output of processed data elements; and

(g) storing the second portion of processed data elements until all of the first portion of data elements is processed;

(h) repeating steps (c), (d), (e), (f) and (g) as necessary until all portions of the data are processed;

(i) transferring the current group of data from each processor 1 to M its corresponding output register 1 to N;

(j) receiving and processing the next group of data within each processor; and simultaneously to (i) and (j),

(k) transferring the portion of data from output register N to output register N-1, the portion of data from output register N-1 to output register N-2, and so on; and

(l) transferring the portion of data from register 1 to a frame buffer.

[c16] 16. The method set forth in Claim 15, wherein the transform is an Inverse Discrete Cosine Transform (IDCT) or an Inverse Differential Quadtree Transform (IDQT).

[c17] 17. The method set forth in Claim 15 wherein each group of data may be represented as row data and column data, and further comprising:

storing the row data while the column data is being processed; and

storing the column data while the row data is being processed.

[c18] 18. The method set forth in Claim 17, further comprising resequencing data elements before the step of storing, such that subsequent delivery of data elements is performed in an efficient manner.

[c19] 19. The method set forth in Claim 15, further comprising controlling each element (a) – (l) based upon predetermined criteria.

[c20] 20. The method set forth in Claim 19, further comprising providing a unique coefficient multiplier to certain data elements based upon predetermined criteria.

[c21] 21. The method set forth in Claim 20, wherein the unique coefficient multiplier is based on E.G. Lee's algorithm.

[c22] 22. The method set forth in Claim 15, wherein the mathematical operation is from the group consisting of addition, multiplication, and subtraction.

[c23] 23. The method as set forth in Claim 15, wherein each butterfly processor performs a portion of a one-dimensional transform.

[c24] 24. The method as set forth in Claim 15, wherein the transform of a block of encoded data is computed as a series of one-dimensional transforms.

[c25] 25. The method as set forth in Claim 14, where M and N are 6.

[c26] 26. The method set forth in Claim 14, further comprising

(m) saturating each portion of the current group of data.

[c27] 27. In a system having a plurality of processors 1 to M, each processor having a corresponding output register 1 to N configurable to receive and transfer data, the data comprising a current group of data and a next group of data, each group comprising a plurality of portions of data, an apparatus configured to transfer data comprising:

means for transferring the current group of data from each processor 1 to M its corresponding output register 1 to N;

means for receiving and processing the next group of data within each processor; and

simultaneously,

means for transferring the portion of data from output register N to output register N-1, the portion of data from output register N-1 to output register N-2, and so on; and

means for transferring the portion of data from register 1 to a frame buffer.

[c28] 28. The apparatus set forth in Claim 27, further comprising means for saturating each portion of the current group of data.

[c29] 29. In a system having a plurality of processors 1 to M, each processor having a corresponding output register 1 to N configurable to receive and transfer data, an apparatus to determine an inverse transform of a block of encoded data, the block of encoded data comprising a first group of data and a next group of data, each group comprising a plurality of data elements, the apparatus comprising:

(a) means for receiving a predetermined quantity of data elements;

(b) means for performing at least one mathematical operation on selected pairs of data elements to produce an output of processed data elements;

(c) means for making a determination as to whether any of the processed data elements require additional mathematical operations;

(d) means for selecting a first portion of processed data elements that require additional mathematical operations;

(e) means for selecting a second portion of processed data elements that do not require additional mathematical operations;

(f) means for performing at least one mathematical operation on selected pairs of the first portion of processed data elements to produce a second output of processed data elements; and

(g) means for storing the second portion of processed data elements until all of the first portion of data elements is processed;

(h) means for repeating steps (c), (d), (e), (f) and (g) all portions of the data are processed;

(i) means for transferring the current group of data from each processor 1 to M its corresponding output register 1 to N;

(j) means for receiving and processing the next group of data within each processor; and simultaneous to (i) and (j),

(k) means for transferring the portion of data from output register N to output register N-1, the portion of data from output register N-1 to output register N-2, and so on; and

(l) means for transferring the portion of data from register 1 to a frame buffer.

[c30] 30. The apparatus set forth in Claim 29, wherein the transform is an Inverse Discrete Cosine Transform (IDCT) or an Inverse Differential Quadtree Transform (IDQT).